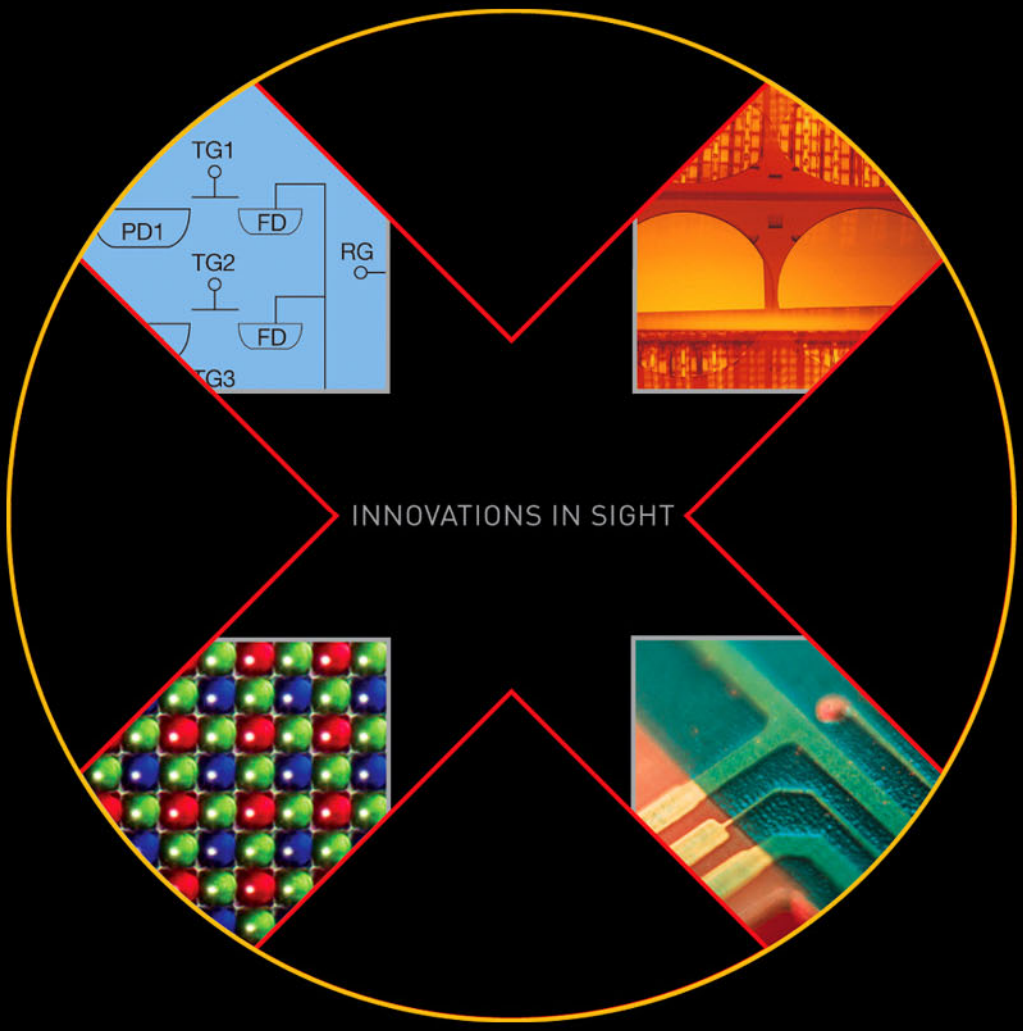
DEVICE PERFORMANCE SPECIFICATION

Revision 2.0 MTD/PS-0996

March 14, 2007



KODAK KAF-8300 IMAGE SENSOR

3326 (H) X 2504 (V) FULL FRAME CCD IMAGE SENSOR

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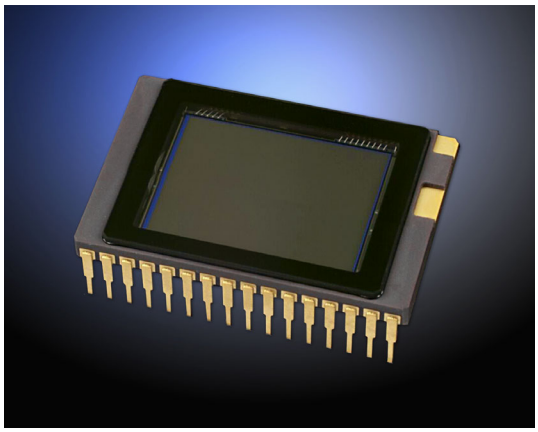
SUMMARY SPECIFICATION

KODAK KAF-8300 IMAGE SENSOR

3326 (H) X 2504 (V) FULL FRAME CCD IMAGE SENSOR

DESCRIPTION

The KODAK KAF-8300 Image Sensor is a 22.5mm diagonal (Four Thirds Format) high performance color or monochrome full frame CCD (charge-coupled device) image sensor designed for a wide range of image sensing applications including digital imaging. Each pixel contains blooming protection by means of a lateral overflow drain thereby preventing image corruption during high light level conditions. For the color version, each of the 5.4µm square pixels are patterned with an RGB mosaic color filter with overlying microlenses for improved color response and reproduction. Several versions of monochrome devices are available with or without microlenses.



Parameter	Typical Value
Architecture	Full Frame CCD; with Square Pixels
Total Number of Pixels	3448 (H) x 2574 (V) = approx. 8.9M
Number of Effective Pixels	3358 (H) x 2536 (V) = approx. 8.6M
Number of Active Pixels	3326 (H) x 2504 (V) = approx. 8.3M
Pixel Size	5.4µm (H) x 5.4µm (V)
Active Image Size	19.7mm (H) x 15.04mm (V) 22.5mm (diagonal)
Aspect Ratio	4:3
Horizontal Outputs	1
Saturation Signal	> 25.5 K e^-
Output Sensitivity	23 µV/e^-
Quantum Efficiency, color R(600nm), G(540nm), B(480nm)	33%, 40 %, 33%
Quantum Efficiency, monochrome Microlens, clear glass (540nm) Microlens, no glass (540nm) Microlens, AR glass (540nm) No Microlens, clear glass (560nm)	 54% 60% 56% 37%
Total Sensor Noise	16 e^-
Dark Signal	< 200 e^-/s
Dark Current Doubling Temperature	5.8 °C
Linear Dynamic Range	64.4 dB
Linearity Error at 12°C	+/- 10%
Charge Transfer Efficiency	0.999995
Blooming Protection (1ms integration time)	1000x saturation exposure
Maximum Data Rate	28 MHz
Package	32-pin CERDIP, 0.070" pin spacing
Cover Glass	Clear or AR coated, 2sides

Parameters above are specified at T = 60 °C and a data rate of 28 MHz unless otherwise noted

FEATURES

- High Resolution
- High Dynamic Range
- Low Noise Architecture

APPLICATIONS

- Photography
- Industrial Imaging
- Medical Imaging

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ORDERING INFORMATION

Catalog Number	Product Name	Description	Marking Code
4H0827	KAF- 8300-AAB-CB-AA	Monochrome, No Microlens, CERDIP Package (sidebrazed), Clear Cover Glass (no coatings), Standard Grade	KAF-8300XE [Serial Number]
4H0828	KAF- 8300-AAB-CB-AE	Monochrome, No Microlens, CERDIP Package (sidebrazed), Clear Cover Glass (no coatings), Engineering Grade	
4H0927	KAF- 8300-AXC-CB-AA	Monochrome, Microlens, CERDIP Package (sidebrazed), Clear Cover Glass (no coatings), Standard Grade	KAF-8300-AXC [Serial Number]
4H0928	KAF- 8300-AXC-CB-AE	Monochrome, Microlens, CERDIP Package (sidebrazed), Clear Cover Glass (no coatings), Engineering Grade	
4H0929	KAF- 8300-AXC-CP-AA	Monochrome, Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass (no coatings), Standard Grade	KAF-8300-AXC [Serial Number]
4H0930	KAF- 8300- AXC-CP-AE	Monochrome, Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass (no coatings), Engineering Grade	
4H0944	KAF- 8300-AXC-CD-AA	Monochrome, Microlens, CERDIP Package (sidebrazed), Clear Cover Glass with AR coating (both sides), Standard Grade	KAF-8300-AXC [Serial Number]
4H0945	KAF- 8300- AXC-CD-AE	Monochrome, Microlens, CERDIP Package (sidebrazed), Clear Cover Glass with AR coating (both sides), Engineering Grade	
4H0469	KAF- 8300-CXB-CB-AA-Offset	Color (Bayer RGB), Special Microlens, CERDIP Package (sidebrazed), Clear Cover Glass (no coatings), Standard Grade, Offset	KAF-8300CE [Serial Number]
4H0468	KAF- 8300-CXB-CB-AE-Offset	Color (Bayer RGB), Special Microlens, CERDIP Package (sidebrazed), Clear Cover Glass (no coatings), Engineering Grade, Offset	
4H0471	KEB-K0021-KAF- 8300-12Bit-28MHz	Evaluation Board (Complete Kit)	N/A

Please see the User's Manual (MTD/PS-0663) for information on the Evaluation Kit for this part.

Please see ISS Application Note "Product Naming Convention" (MTD/PS-0892) for a full description of naming convention used for KODAK image sensors.

Address all inquiries and purchase orders to:

Image Sensor Solutions
Eastman Kodak Company
Rochester, New York 14650-2010

Phone: (585) 722-4385
Fax: (585) 477-4947
E-mail: imagers@kodak.com

Kodak reserves the right to change any information contained herein without notice. All information furnished by Kodak is believed to be accurate.

DEVICE DESCRIPTION

ARCHITECTURE

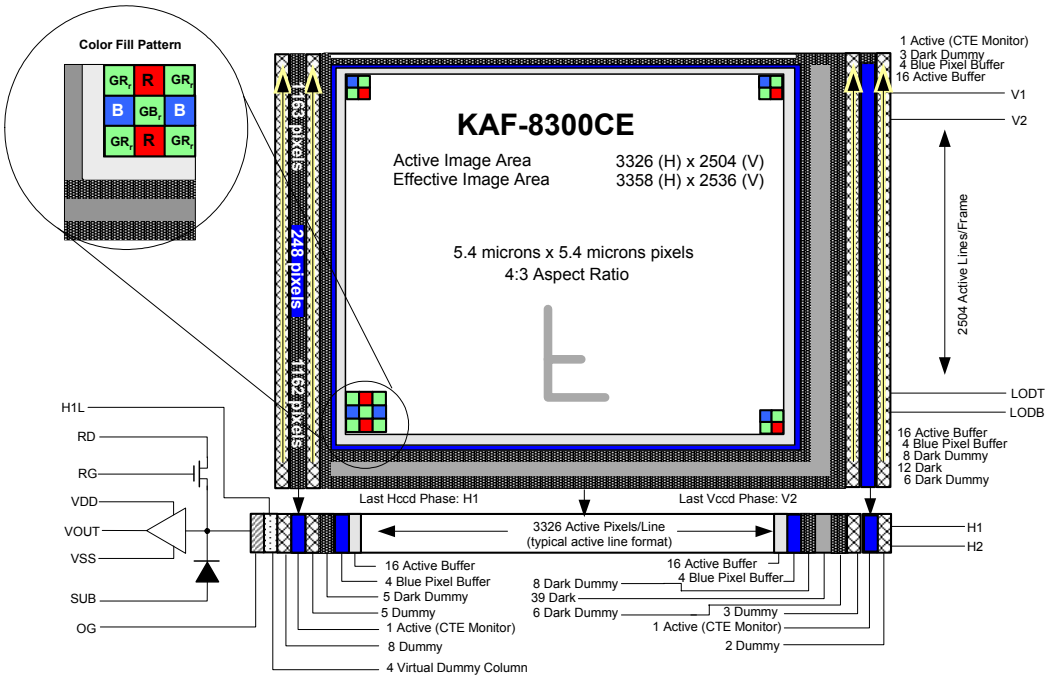

Figure 1: Block Diagram
(showing the color filter pattern. Monochrome version will not have any color pattern.)

Dark Reference Pixels

Surrounding the periphery of the device is a border of light shielded pixels creating a dark region. Within this dark region, exist light shielded pixels that include 39 trailing dark pixels on every line. There are also 12 full dark lines at the start of every frame. Under normal circumstances, these pixels do not respond to light and may be used as a dark reference.

Dark Dummy Pixels

Within the dark region some pixels are in close proximity to an active pixel, or the light sensitive regions that have been added for manufacturing test purposes, (CTE Monitor). In both cases, these pixels can scavenge signal depending on light intensity and wavelength. These pixels should not be used as a dark reference. These pixels are called dark dummy pixels.

Within the dark region, dark dummy pixels have been identified. There are 5 leading and 14 (6 + 8) trailing dark pixels on every line. There are also 14 (6 + 8) dark dummy lines at the start of every frame along with 3 dark dummy lines at the end of each frame

Dummy Pixels

Within the horizontal shift register there are 13, (8 + 5), leading and 5, (2 + 3), trailing additional shift phases that are not electrically associated with any columns of pixels within the vertical register. These pixels contain only horizontal shift register dark current signal and do not respond to light and therefore, have been designated as dummy pixels. For this reason, they should not be used to determine a dark reference level.

Virtual Dummy Columns

Within the horizontal shift register there is 4 leading shift phases that are not physically associated with a column of pixels within the vertical register. These pixels contain only horizontal shift register dark current signal and do not respond to light and therefore, have been designated as virtual dummy columns. For this reason, they also should not be used to determine a dark reference level.

Active Buffer Pixels

Sixteen buffer pixels adjacent to the CTE monitor pixel region contain a RGB mosaic color pattern (in the case of a color device but monochrome version is uncoated). This region is classified as active buffer pixels. These pixels are light sensitive but they are not tested for defects and non-uniformities. The response of these pixels will not be uniform.

Blue Pixel Buffer

Four buffer pixels adjacent to any leading or trailing dark reference regions contain a blue filter (color version only, monochrome version is uncoated). This region is classified as a blue pixel buffer. These pixels are light sensitive but they are not tested for defects and non-uniformities. The response of these pixels will not be uniform.

CTE Monitor Pixels

Within the horizontal dummy pixel region two light sensitive test pixels (one each on the leading and trailing ends) are added and within the vertical dummy pixel region one light sensitive test pixel has been added. These CTE monitor pixels are used for manufacturing test purposes. In order to facilitate measuring the device CTE, the pixels in the CTE Monitor region in the horizontal and vertical portion is coated with blue pigment (color version only, monochrome version is uncoated).

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IMAGE ACQUISITION

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the device. These photon-induced electrons are collected locally by the formation of potential wells at each photogate or pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons are discharged into the lateral overflow drain to prevent crosstalk or 'blooming'. During the integration period, the V1 and V2 register clocks are held at a constant (low) level.

CHARGE TRANSPORT

The integrated charge from each photogate is transported to the output using a two-step process. Each line (row) of charge is first transported from the vertical CCD's to a horizontal CCD register using the V1 and V2 register clocks. The horizontal CCD is presented a new line on the falling edge of V2 while H1 is held high. The horizontal CCD's then transport each line, pixel by pixel, to the output structure by alternately clocking the H1 and H2 pins in a complementary fashion. A separate connection to the last H1 phase (H1L) is provided to improve the transfer speed of charge to the floating diffusion. On each falling edge of H1 a new charge packet is dumped onto a floating diffusion and sensed by the output amplifier.

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HORIZONTAL REGISTER

Output Structure

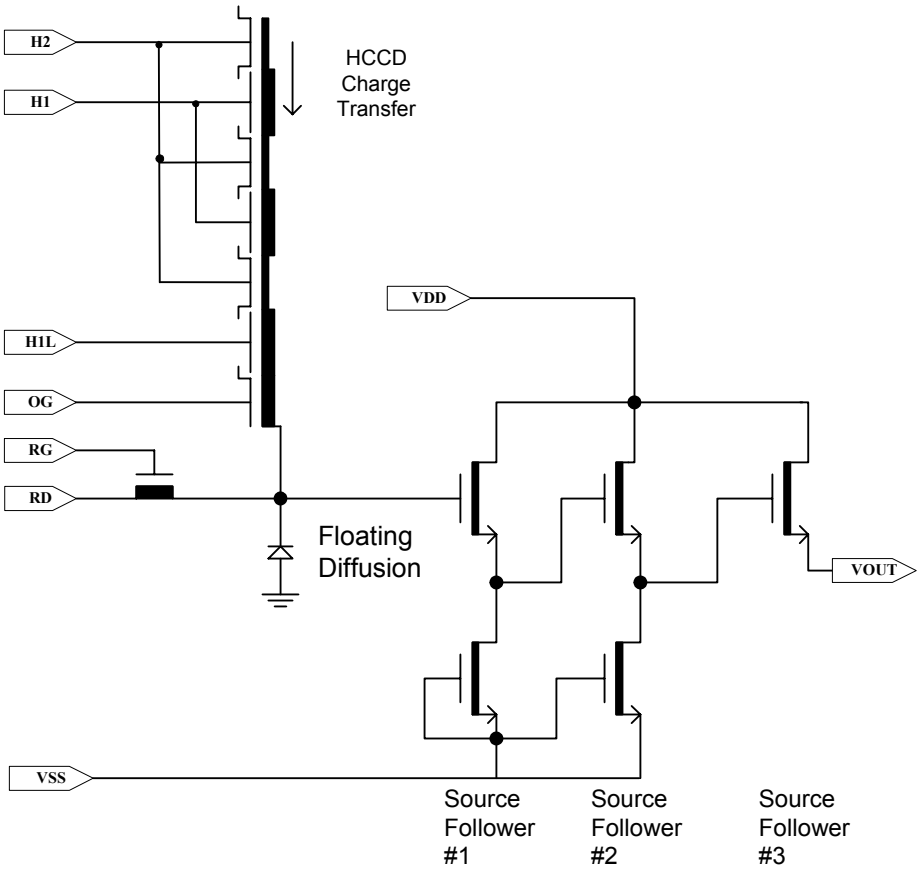

Figure 2: Output Architecture (Left or Right)

Charge presented to the floating diffusion (FD) is converted into a voltage and is current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on the FD. Once the signal has been sampled by the system electronics, the reset gate (RG) is clocked to remove the signal and FD is reset to the potential applied by reset drain (RD). Increased signal at the floating diffusion reduces the voltage seen at the output pin. To activate the output structure, an off-chip load must be added to the VOUT pin of the device. See Figure 3.

.

Output Load

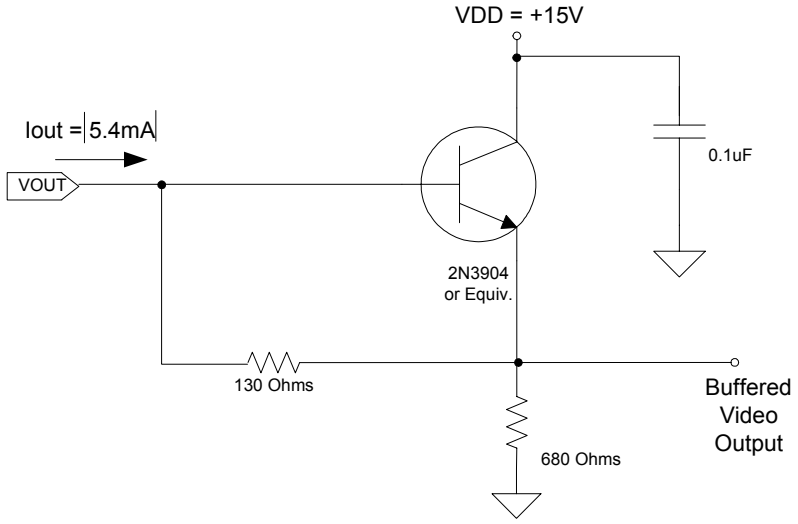

Figure 3: Recommended Output Structure Load Diagram

Component values may be revised based on operating conditions and other design considerations.

PHYSICAL DESCRIPTION

Pin Description and Device Orientation

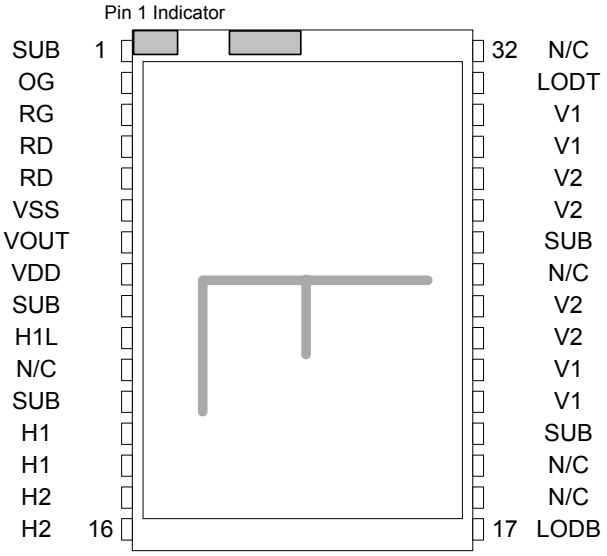

Figure 4: Pinout Diagram

Pin	Name	Description
1	SUB	Substrate
2	OG	Output Gate
3	RG	Reset Gate
4	RD	Reset Drain Bias
5	RD	Reset Drain Bias
6	VSS	Output Amplifier Return
7	VOUT	Output
8	VDD	Output Amplifier Supply
9	SUB	Substrate
10	H1L	Horizontal Phase 1, Last Gate
11	N/C	No Connection
12	SUB	Substrate
13	H1	Horizontal Phase 1
14	H1	Horizontal Phase 1
15	H2	Horizontal Phase 2
16	H2	Horizontal Phase 2

Pin	Name	Description
32	N/C	No Connection
31	LODT	Lateral Overflow Drain Top
30	V1	Vertical Phase 1
29	V1	Vertical Phase 1
28	V2	Vertical Phase 2
27	V2	Vertical Phase 2
26	SUB	Substrate
25	N/C	No Connection
24	V2	Vertical Phase 2
23	V2	Vertical Phase 2
22	V1	Vertical Phase 1
21	V1	Vertical Phase 1
20	SUB	Substrate
19	N/C	No Connection
18	N/C	No Connection
17	LODB	Lateral Overflow Drain Bottom

Note: Wherever possible, all N/C pins (11, 18, 19, 25, 32) should be connected to GND (0V).

IMAGING PERFORMANCE

TYPICAL OPERATIONAL CONDITIONS

Description	Condition - Unless otherwise noted	Notes
Readout Time ($t_{readout}$)	370.36 msec	Includes tVoverclock & tHoverclock
Integration time (tint)	33 msec	
Horizontal clock frequency	28 MHz	
Light source (LED)	Red, green, blue, orange	
Mode	Flush – integrate – readout cycle	

SPECIFICATIONS

Monochrome and Color Versions

Description	Symbol	Min.	Nom.	Max	Units	Notes	Sample Plan[18]
Minimum Column	MinColumn	575			mV	1	die
Linear Saturation Signal	Ne^-_{sat}	25.5K			e^-	1,3	design
Charge to Voltage Conversion	Q-V	22.5	23		$\mu V/e^-$		design
Linearity Error	LeLow10 LeLow33 LeHigh	-10 -10 -10		10 10 10	% % %	2,5,6 2,5,6 2,5	die die die
Dark Signal (Active Area Pixels)	AA_DarkSig			200	e-/s	8	die
Dark Signal (Dark Reference Pixels)	DR_DarkSig			200	e-/s	8	die
Readout Cycle Dark Signal	Dark_Read			15	mV/s		die
Flush Cycle Dark Signal	Dark_Flush		43	90	mV/s		die
Dark Signal Non-Uniformity	DSNU DSNU_Step DSNU_H		1.30 0.14 0.4	3 0.5 1.0	mVp-p mV p-p mVp-p	9 9 9	die die die
Dark Signal Doubling Temperature	ΔT		5.8		°C		design
Dark Reference Difference, Active Area	DarkStep	-3.5	0.15	3.5	mV		die
Total Noise	Dfld_noi			1.08	mV	10	die
Total Sensor Noise	N		16		e^- rms	19	design
Linear Dynamic Range	DR		64.4		dB	11	design
Horizontal Charge Transfer Efficiency	HCTE	0.999990	0.999995			13, 21	die
Vertical Charge Transfer Efficiency	VCTE	0.99997	0.999999		%	21	die
Blooming Protection	X_b	1000			x Esat	14	design
Vertical Bloom on Transfer	VBloomF	-20		20	mV		die
Horizontal Crosstalk	H_Xtalk	-20		20	mV		die
Horizontal Overclock Noise	Hoclk_noi	0		1.08	mV		die

Monochrome and Color Versions (Continued)

Description	Symbol	Min.	Nom.	Max	Units	Notes	Sample Plan[18]
Output Amplifier Bandwidth	f_{-3dB}	88		159	Mhz	6,16	die
Output Impedence, Amplifier	R_{OUT}	100		180	Ohms		die
Hclk Feedthru	V_{hft}			70	mV	17	die
Reset Feedthru	V_{rft}	500	710	1000	mV		design

Color Version Only

Description	Symbol	Min.	Nom.	Max	Units	Notes	Sample Plan[18]
Sensitivity red, green, blue	 Rresp Gresp Bresp	 260 442 230		 420 638 420	 mV mV mV		 die die die
QE R(600nm) G(540nm) B(480nm)	 QE, red QE green QE, blue		 33 40 33		%		design
Off-band Response Green inband, Red response Blue response Red inband, Green response Blue response Blue inband, Red response Green response	 Gr_Gresp Gr_Rresp Gr_Bresp Rd_Rresp Rd_Gresp Rd_Bresp Bl_Bresp Bl_Rresp Bl_Gresp	 362 0 0 180 0 0 90 0 0		 630 130 260 430 120 45 420 40 120	 mV mV mV mV mV mV mV mV mV		 die die die die die die die die die
Linearity Balance	Red_Bal Blu_Bal	-14 -8	6.4 0.2	14 8	% %	2, 6 2, 6	die die
Photo Response Non-Uniformity	R_PRNU G_PRNU B_PRNU			15 15 15	%p-p %p-p %p-p	7 7 7	die die die
High Frequency Noise	R_Nois GRr_Nois GBr_Nois B_Nois			2 2 2 2	%rms %rms %rms %rms		die die die die
Red-Green Hue Shift	RGHueUnif			10	%	12	die
Blue-Green Hue Shift	BGHueUnif			12	%	12	die
GRr/GBr Hue Uniformity	GrGbHueUnf			7	%	12	die
Green Light GRr/GBr Hue Uniformity	Gr_GHueUnf			9	%		die
Low Hue Uniformity	RGLoHueUnf BGLoHueUnf			12 10	% %		die die
Streak/Spot	GrnStreak RedStreak BluStreak			40 20 20	% % %		

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Color Version Only (Continued)

Description	Symbol	Min.	Nom.	Max	Units	Notes	Sample Plan[18]
Local Green Difference							
white light, min	W_GNU_Min			4	%		die
white light, max	W_GNU_Max			6	%		die
green light, min	Gr_GNU_Min			4	%		die
green light, max	Gr_GNU_Max			4	%		die
red light, min	R_GNU_Min			65	%		die
red light, max	R_GNU_Max			65	%		die
blue light, min	B_GNU_Min			40	%		die
blue light, max	B_GNU_Max			40	%		die
Chroma Test	UL_Chroma			7	%		die
	UR_Chroma			7	%		die
	LL_Chroma			7	%		die
	LR_Chroma			7	%		die
Hue Test	UL_UR_Hue			6	%		die
	UL_LR_Hue			6	%		die
	UL_LL_Hue			6	%		die
	UR_LR_Hue			6	%		die
	UR_LL_Hue			6	%		die
	LR_LL_Hue			6	%		die

Monochrome Versions Only

Description	Symbol	Min.	Nom.	Max	Units	Notes	Sample Plan[18]
Sensitivity Monochrome	Resp	465		655	mV		die
QE							
Microlens, clear glass (540nm)	QE		54%		%		design
Microlens, no glass (540nm)			60%				
Microlens, AR glass (540nm)			56%				
No Microlens, clear glass (560nm)			37%				

Notes:

1. Increasing output load currents to improve bandwidth will decrease these values.
2. Specified from 12C to 60C.
3. Saturation signal level achieved while meeting Le specification. Specified from 0ºC to 40ºC.
4. This note left blank
5. Worst case deviation, (from 10mV to Vsat min), relative to a linear fit applied between 0 and 500mV exposure.
6. Tested at T=25°C.
7. Peak to peak non-uniformity test based on an average of 185 x 185 blocks.
8. Average non-illuminated signal with respect to over clocked horizontal register signal.
9. Absolute difference between the maximum and minimum average signal levels of 185 x 185 blocks within the sensor.
10. Dark rms deviation of a multi-sampled pixel as measured using the KAF-8300CE Evaluation Board.
11. 20log(Vsat/N)
12. Gradual variations in hue (red with respect to green pixels and blue with respect to green

pixels) in regions of interest of 185 x 185 blocks.

13. Measured per transfer at 80% of Vsat.

14. Esat equals the exposure required to achieve saturation. X_b represents the number of Esat exposures the sensor can tolerate before failure. X_b characterized at 25 °C.

15. Video level DC offset with respect to ground at clamp position. Refer to Pixel Timing Diagram Figure 15.

16. Last stage only. CLOAD = 10pF. Then f-3dB = (1 / (2p*ROUT*CLOAD)).

17. Amount of artificial signal due to H1 coupling.

18. Sampling plan defined as "die" indicates that every device is verified against the specified performance limits. Sampling plan defined as "design" indicates a sampled test or characterization, at the discretion of Kodak, against the specified performance limits.

19. Calculated value subtracting the noise contribution from the KAF-8300CE Evaluation Board.

20. Process optimization has effectively eliminated vertical striations.

21. CTE = 1 - CTI. Where CTE is charge transfer efficiency and CTI is charge transfer inefficiency. CTI is the measured value

TYPICAL PERFORMANCE CURVES

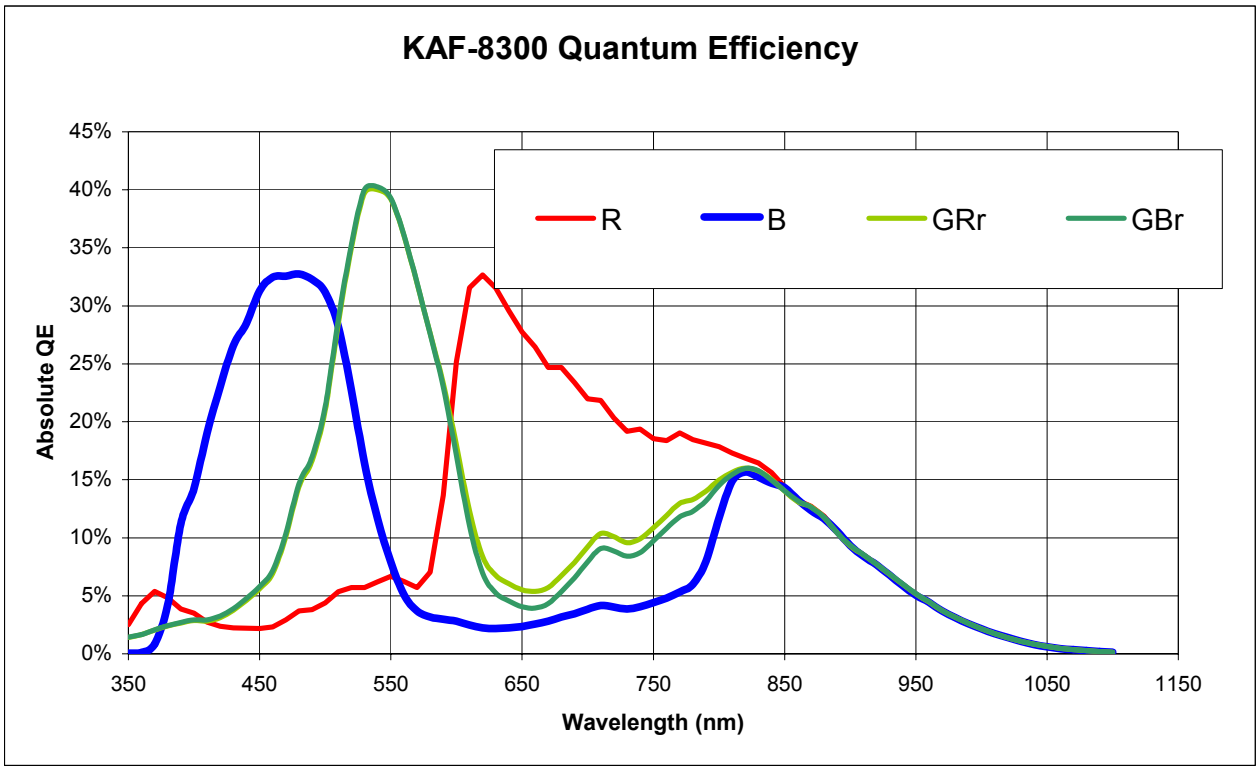

Figure 5: Typical Quantum Efficiency, Color version

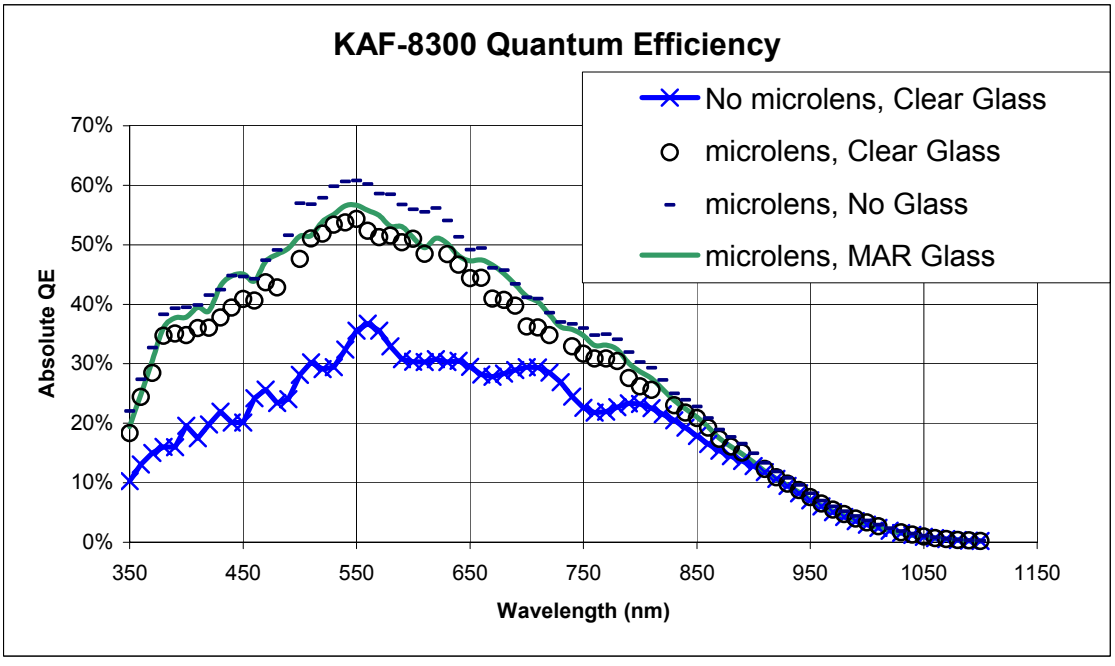

Figure 6: Typical Quantum Efficiency, all Monochrome versions

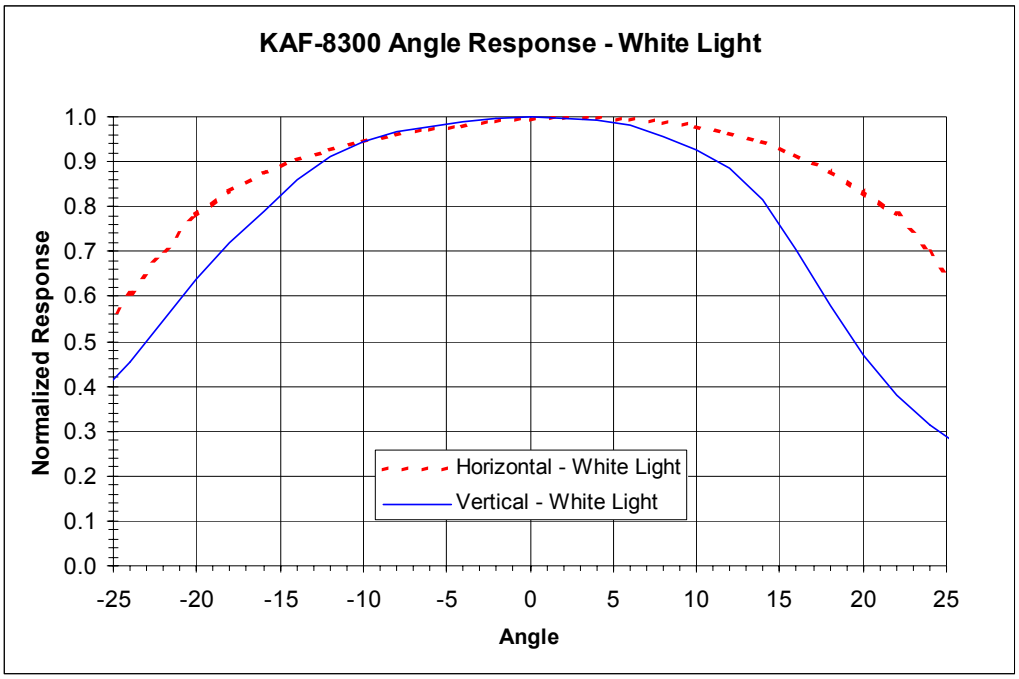

Figure 7: Typical Angular Response, Color version
(Center location of die as shown. Effective optical shift is 6° center-to-edge, along diagonal.)

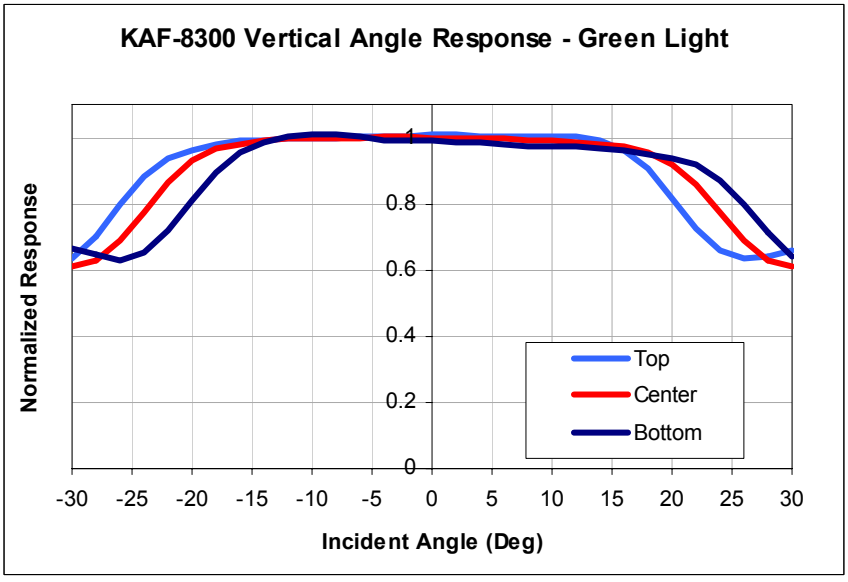

Figure 8: Typical Angular Response, Monochrome with microlens
(Effective optical shift is 6° center-to-edge, along diagonal.)

DEFECT DEFINITIONS

OPERATIONAL CONDITIONS

The Defect Specifications are measured using the following conditions:

Description	Test Condition	Notes
Integration time (tint)	33 msec	Unless otherwise noted

SPECIFICATIONS

Monochrome and Color Versions

Description	Symbol	Definition	Threshold	Maximum Number Allowed
Point defect	BPnt33_7	Dark field, minor, short integration time	7.5 mV	800 total Points allowed for this group of tests
Point defect	Bfld_Pnt_D	Dark point in an illuminated field	11%	
Point defect	Bfld_Pnt_B	Bright point in an illuminated field	7%	
Point defect	BPnt33_100	Dark field, major, short integration time	100 mV	
Point defect	BPnt33_500	Dark field, major, short integration time	500 mV	0
Point defect	BPnt333_13	Dark field, minor, long integration time, tint=1/3 sec	13 mV	32,500[1]
Point Defect	DR_BPnts	Bright point in the dark reference region	7.5 mV	0
Cluster defect	Total_Clst	A cluster is a group of 2 or more defective pixels that do not exceed the perpendicular pattern defect.	---	6 total
Cluster defect	Dfld_Vperp	Dark field very long exposure bright cluster where 9 or more adjacent point defects exist, very long integration time, tint=1 sec	3.04 mV	0
Cluster Defect – Perpendicular Pattern Defect	Dfld_Perp Bfld_Perp Total_Perp	Three or more adjacent point defects in the same color plane, along a row or column.[2]	---	0
Column defect, illuminated	Bfld_Col_D Bfld_Col_B	A column which deviates above or below neighboring columns under illuminated conditions (>300mV signal) greater than the threshold	1.5% 1.5%	0
Column defect, darkfield	Dfld_Col2 Dfld_Col4 Lo_Col_B Lo_Col_D Lo_Col_B1 Lo_Col_D1	A column which deviates above or below neighboring columns under non-illuminated or low light level conditions (~10mV) greater than the threshold	1 mV 1 mV 1 mV 1 mV 1 mV 1 mV	0
Row Defect	Dfld_Row	Row defect if row average deviates above threshold	1 mV	0
Streak Test, dark	DarkStreak	Maximum defect density gradient allowed in the entire imaging area.	40%	0
LOD Bright Col, dark	Dfld_LodCol	Defines functionality and uniform efficiency of LOD structure	1.5 mV	0

Color Version Only

Description	Symbol	Definition	Threshold	Maximum Number Allowed
Streak Test, color	GrnStreak RedStreak BluStreak	Maximum defect density gradient allowed in a color bit plane.[4]	40% 20% 20%	0

Notes:

1. This parameter is only a quality metric and these points will not be considered for cluster and point criteria.
2. For the color version of this device, the green pixels in a red row (GR) are considered a different color plane than the green pixels in a blue row (GB). For monochrome version the entire active area is treated as a single color plane.
3. This note left blank.
4. As the gradient threshold is defined as 8.5 mV maximum across a 16 x 16 pixel region about each pixel. 5. As the gradient threshold is defined as 6 mV maximum across a 50 x 50 pixel region about each pixel.

OPERATION

ABSOLUTE MAXIMUM RATINGS

Description[9]	Symbol	Minimum	Maximum	Units	Notes
Diode Pin Voltages	V_{diode}	-17.5	+17.5	V	1,2
Gate Pin Voltages	V_{gate1}	-13.5	+13.5	V	1,3
Overlapping Gate Voltages	V_{1-2}	-13.5	+13.5	V	4
Non-overlapping Gate Voltages	V_{g-g}	-13.5	+13.5	V	5
V1, V2 – LOD Voltages	VV_{VL}	-13.5	+13.5	V	6
Output Bias Current	I_{out}		-30	mA	7
LODT Diode Voltage	V_{LODT}	-13.0	+13.0	V	8
LODB Diode Voltage	V_{LODB}	-18.0	+18.0	V	8
Operating Temperature	T_{OP}	-10	70	oC	10
Guaranteed Temperature of Performance	T_{SP}	0	60	°C	11

Notes:

1. Referenced to pin SUB
2. Includes pins: RD, VDD, VSS, and VOUT.
3. Includes pins: V1, V2, H1, H1L, H2, RG, OG.
4. Voltage difference between overlapping gates. Includes: V1 to V2; H1, H1L to H2; H1L to OG; V1 to H2.
5. Voltage difference between non-overlapping gates. Includes: V1 to H1, H1L; V2, OG to H2.
6. Voltage difference between V1 and V2 gates and LODT, LODB diode.
7. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher currents and lower load capacitance at the expense of reduced gain (sensitivity). Operation at these values will reduce MTTF.
8. V1, H1, V2, H2, H1L, OG, and RD are tied to 0V.
9. Absolute maximum rating is defined as a level or condition that should not be exceeded at any time per the description. If the level or condition is exceeded, the device will be degraded and may be damaged.
10. Noise performance will degrade at higher temperatures.
11. See section for Imaging Performance Specifications.

POWER-UP SEQUENCE

The sequence chosen to perform an initial power-up is not critical for device reliability. A coordinated sequence may minimize noise and the following sequence is recommended:

1. Connect the ground pins (SUB).
2. Supply the appropriate biases and clocks to the remaining pins.

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DC BIAS OPERATING CONDITIONS

Description	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current (mA)	Notes
Reset Drain	RD	11.3	11.5	11.7	V	IRD = 0.01	
Output Amplifier Return	VSS	1.05	1.25	1.45	V	ISS = -3.0	
Output Amplifier Supply	VDD	14.5	15.0	15.5	V	IOUT + ISS	
Substrate	SUB		GND		V	-0.01	2
Output Gate	OG	-3	-2.8	-2.6	V	0.1	
Lateral Drain	LODT, LODB	9.5	9.75	10.0	V	0.2	2
Video Output Current	I_{OUT}	-3	-5	-8	mA		1

Notes:

1. An output load sink must be applied to VOUT to activate output amplifier – see Figure 3.
2. Maximum current expected up to saturation exposure (Esat).

AC OPERATING CONDITIONS

Clock Levels

Description	Symbol	Level	Minimum	Nominal	Maximum	Units	Effective Capacitance	Notes
V1 Low Level	V1L	Low	-9.5	-9.25	-9.0	V	76 nF	1
V1 High Level	V1H	High	2.4	2.6	2.85	V		1
V2 Low Level	V2L	Low	-9.5	-9.25	-9.0	V	81 nF	1
V2 High Level	V2H	High	2.4	2.6	2.8	V		1
RG, H1, H2, amplitude	RG_{amp} $H1_{amp}$ $H2_{amp}$	Amp	5.5	6.0	6.5	V	RG = 7 pF H1 = 224 pF H2 = 168 pF	1
H1L, amplitude	$H1_{Lamp,}$	Amp	7.5	8.0	8.5	V	7 pF	1
H1 Low Level	$H1_{low,}$	Low	-4.7	-4.5	-4.3	V		1
H1L Low Level	$H1L_{low}$	Low	-6.7	-6.5	-6.3	V		
H2 Low Level	$H2_{low}$	Low	-5.2	-5	-4.8	V		
RG Low Level	RG_{low}	Low	1.8	2.0	2.2	V		1

Note:

1. All pins draw less than 10mA DC current. Capacitance values relative to SUB (substrate).

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Clock Voltage Detail Characteristics

(Note 1)

Description	Symbol	Min	Nom	Max	Units	Notes
V1 High-level variation	$V1_{HH}$	-	0.50	1	V	High-level coupling
V2 High-level variation	$V2_{HL}$	-	0.28	1	V	High-level coupling
V2 Low-level variation	$V2_{LH}$	-	0.46	1	V	Low-level coupling
V1 Low-level variation	$V1_{LL}$	-	0.14	1	V	Low-level coupling
V1-V2 Cross-over	$V1_{CR}$	-2	-0.5	1	V	Referenced to ground
H1 High-level variation	$H1_{HH}$	-	0.30	1	V	
H1 High-level variation	$H1_{HL}$	-	0.07	1	V	
H1 Low-level variation	$H1_{LH}$	-	0.16	1	V	
H1 Low-level variation	$H1_{LL}$	-	0.25	1	V	
H2 High-level variation	$H2_{HH}$	-	0.40	1	V	
H2 High-level variation	$H2_{HL}$	-	0.06	1	V	
H2 Low-level variation	$H2_{LH}$	-	0.10	1	V	
H2 Low-level variation	$H2_{LL}$	-	0.27	1	V	
H1 – H2 Cross-over	$H1_{CR1}$	-3	-1.23	0	V	Rising side of H1
H1 – H2 Cross-over	$H1_{CR2}$	-3	-0.59	0	V	Falling side of H1
H1L High-level variation	$H1L_{HH}$	-	0.64	1	V	
H1L High-level variation	$H1L_{HL}$	-	0.32	1	V	
H1Llow-level variation	$H1L_{LH}$	-	0.27	1	V	
H1Llow-level variation	$H1L_{LL}$	-	0.23	1	V	
H1L – H2 Cross-over	$H1L_{CR1}$	-1	-	-3	V	Rising side of H1L
RG High-level variation	RG_{HH}	-	0.19	1	V	
RG High-level variation	RG_{HL}	-	0.20	1	V	
RG Low-level variation	RG_{LH}	-	0.11	1	V	
RG Low-level variation	RG_{LL}	-	0.30	1	V	

Notes:

1. H1, H2 clock frequency: 28MHz. The maximum and minimum values in this table are supplied for reference. The actual clock levels were measured using the KAF-8300CE Evaluation Board. Testing against the device performance specifications is performed using the nominal values.

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CAPACITANCE EQUIVALENT CIRCUIT

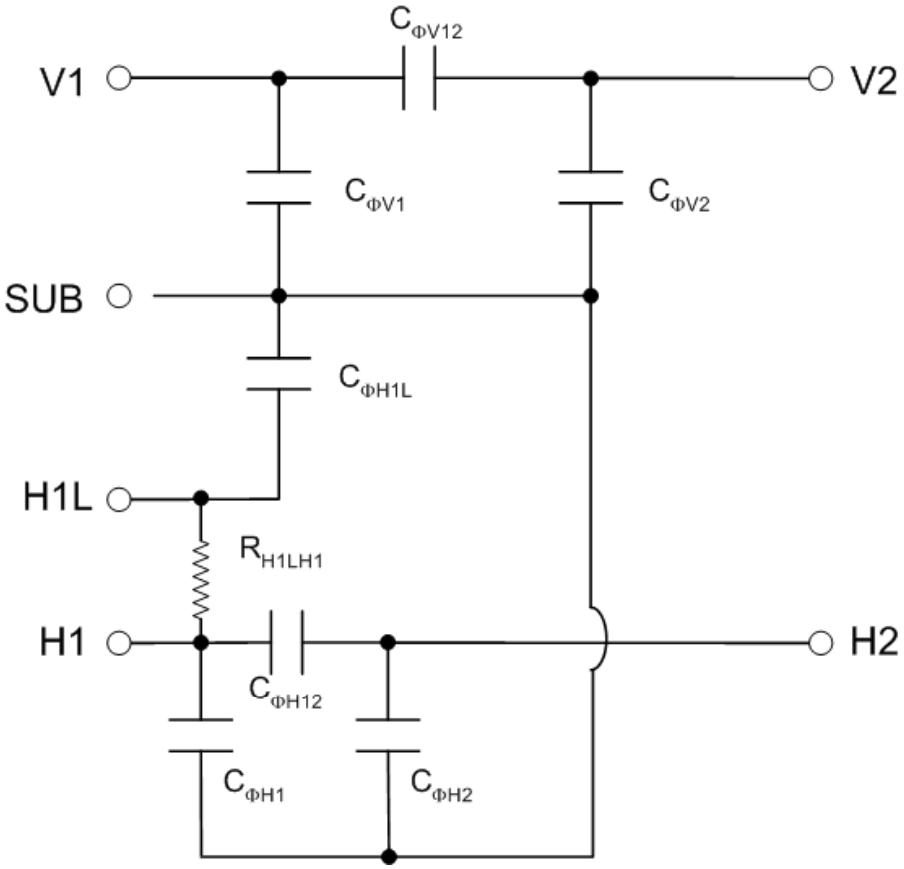

Figure 9: Equivalent Circuit Model
The external pin names are actual pins on this image sensor. See the pinout diagram (Figure 4) for more information.
The components shown in this schematic model do not correspond to actual components inside the image sensor.

Parameter	Value (typical)	Units
$C_{\Phi V1}$	61	nF
$C_{\Phi V12}$	15	nF
$C_{\Phi V2}$	67	nF
$C_{\Phi H1}$	153	nF
$C_{\Phi H12}$	36	nF
$C_{\Phi H2}$	97	nF
$C_{\Phi H1L}$	7	nF
R_{H1LH1}	52	Kohms

TIMING

REQUIREMENTS AND CHARACTERISTICS

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
H1, H2 Clock Frequency	f_H			28	MHz	1, 2
V1, V2 Clock Frequency	f_V			125	kHz	2
Pixel Period (1 Count)	t_e	35.7			ns	2
H1, H2 Setup Time	t_{HS}	1			ms	
H1L – VOUT Delay	t_{HV}		3		ns	
RG – VOUT Delay	t_{RV}		1		ns	
Readout Time	$t_{readout}$	340.2			ms	4, 5
Integration Time	t_{int}					3, 4
Line Time	t_{line}	132.2			ms	4
Flush Time	t_{flush}	21.23			ms	6

Notes:

1. 50% duty cycle values.
2. CTE will degrade above the nominal frequency.
3. Integration time is user specified.
4. Longer times will degrade noise performance.
5. treadout = tline * 2574 lines.
6. See Figure 17 for a detailed description.

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Clock Switching Characteristics

(Note 1)

Description	Symbol	Min	Nom	Max	Units	Notes
V1 Rise Time	t_{V1r}	-	0.26	1	us	3
V2 Rise Time	t_{V2r}	-	0.55	1	us	3
V1 Fall Time	t_{V1f}	-	0.43	1	us	3
V2 Fall Time	t_{V2f}	-	0.31	1	us	3
V1 Pulse Width	t_{V1w}	5.0	-	-	us	4, 5
V2 Pulse Width	t_{V2w}	3.0	-	-	us	4, 5
H1 Rise Time	t_{H1r}	-	9.0	10	ns	3
H2 Rise Time	t_{H2r}	-	6.9	10	ns	3
H1 Fall Time	t_{H1f}	-	5.8	10	ns	3
H2 Fall Time	t_{H2f}	-	5.4	10	ns	3
H1 – H2 Pulse Width	t_{H1w}, t_{H2w}	14	18	22	ns	
H1L Rise Time	t_{H1Lr}		1.8	4	ns	3
H1L Fall Time	t_{H1Lf}		2.5	4	ns	3
H1L Pulse Width	t_{H1Lw}	14	19.0	22	ns	
RG Rise Time	t_{RGr}	-	2.0	4	ns	3
RG Fall Time	t_{RGf}	-	2.2	4	ns	3
RG Pulse Width	t_{RGw}	-	6.7	-	ns	2

Notes:

1. H1, H2 clock frequency: 28MHz. The maximum and minimum values in this table are supplied for reference. The actual clock timing was measured using the KAF-8300CE Evaluation Board. Testing against the device performance specifications is performed using the nominal values.
2. RG should be clocked continuously.
3. Relative to the pulse width (based on 50% of high/low levels).
4. CTE
5. Longer times will degrade noise performance.

EDGE ALIGNMENT

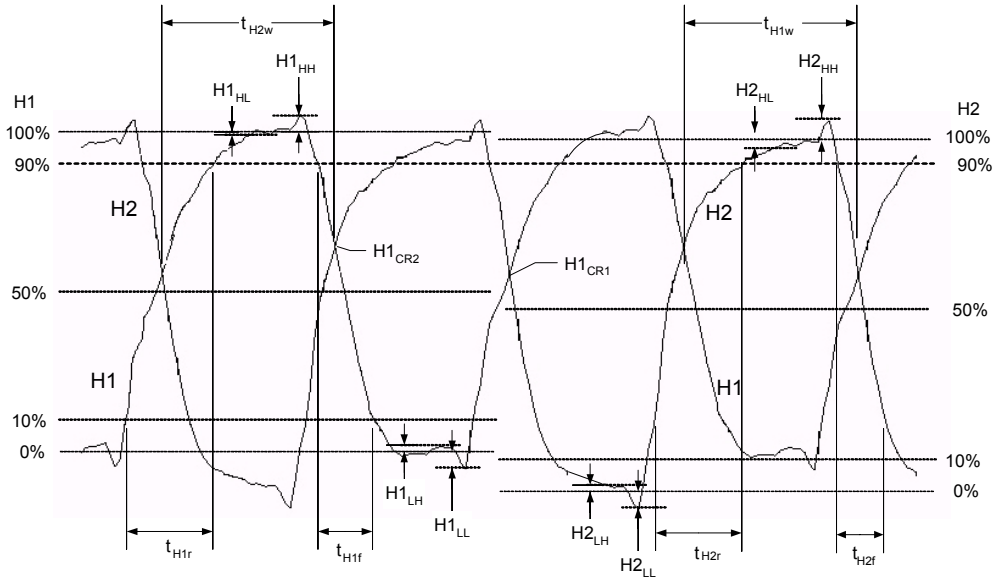

Figure 10: H1 and H2 Edge Alignment

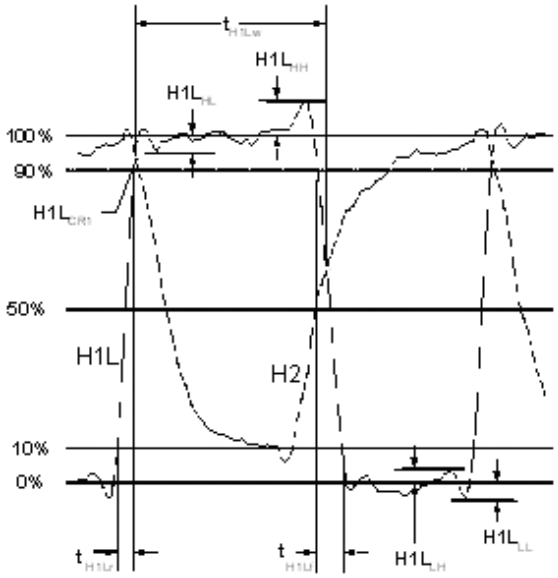

Figure 11: H1L and H2 Edge Alignment

FRAME TIMING

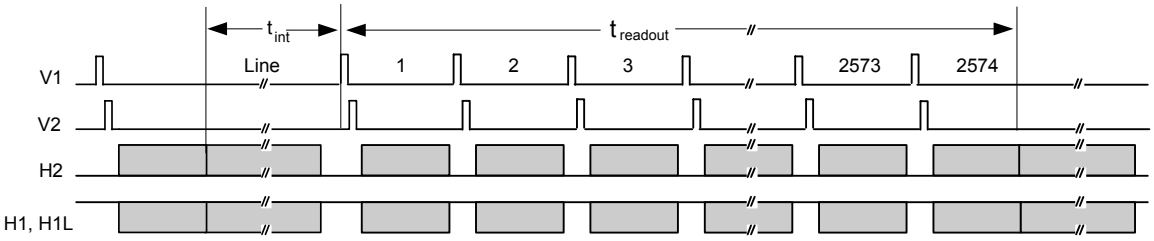

Figure 12: Frame Timing (minimum)

Frame Timing Detail

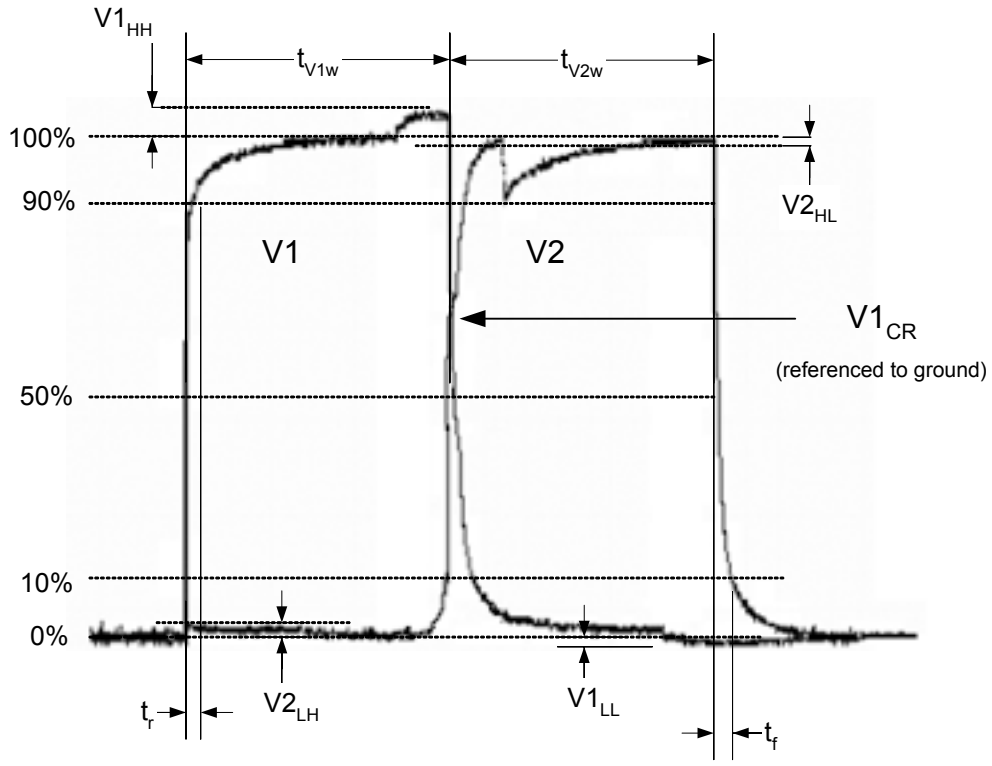

Figure 13: Frame Timing Edge Alignment

LINE TIMING

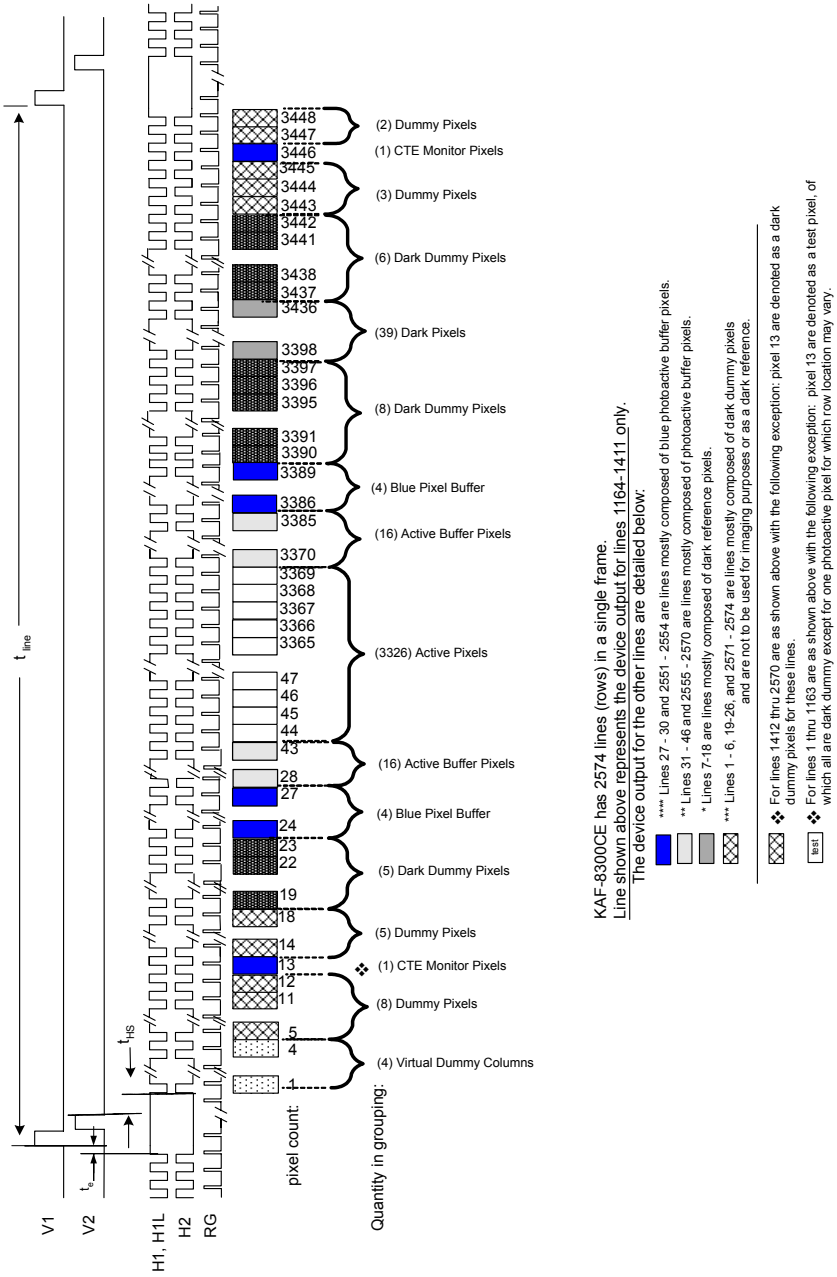

Figure 14: Line Timing

Schematic reference regions that contain a blue filter represent the color version only; monochrome version is uncoated for these pixels.

PIXEL TIMING

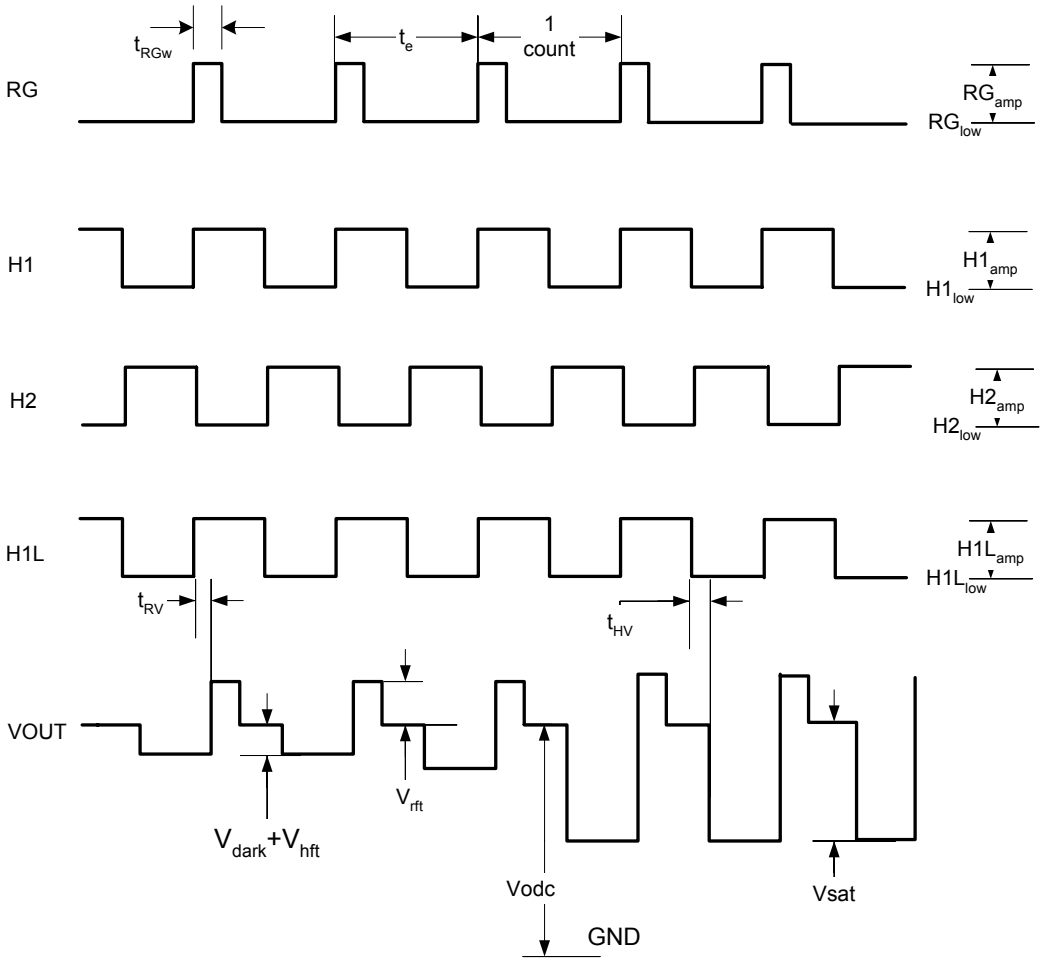

Figure 15: Pixel Timing

Pixel Timing Detail

RG

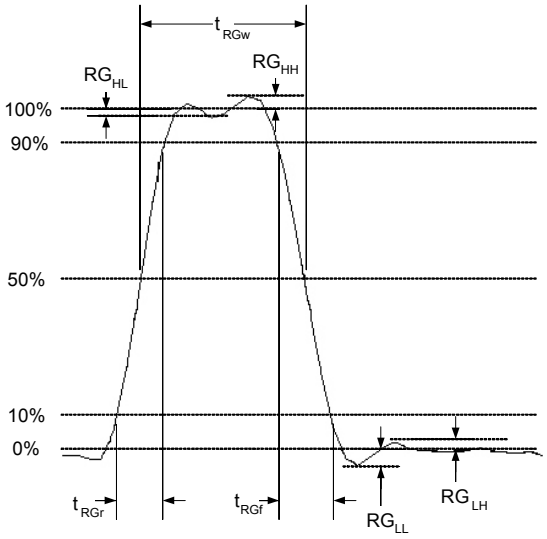

Figure 16: Pixel Timing Detail

MODE OF OPERATION

POWER-UP FLUSH CYCLE

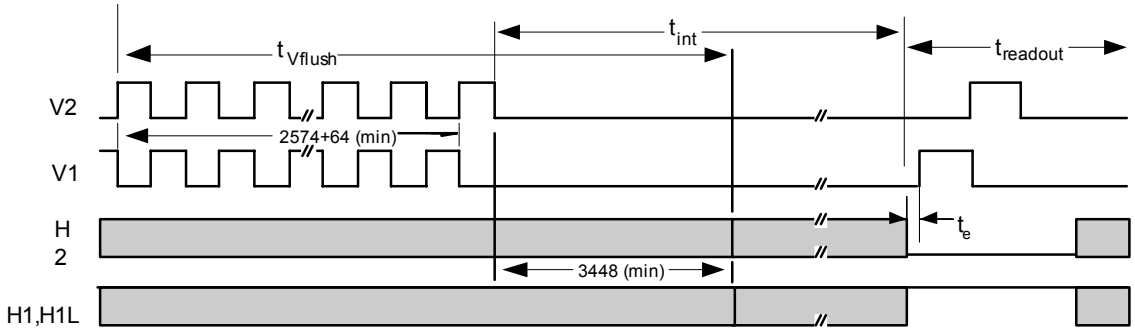

Figure 17: Power-up Flush Cycle

STORAGE AND HANDLING

STORAGE CONDITIONS

Short Term Storage (< 1 year storage)

Assembled devices, in their first level packing container, should be stored indoors, in a dust-free, enclosed environment with the conditions described in the table below. The first level packing includes the tray and a single barrier bag. A fully-sealed bag under vacuum not necessary. Purpose of the barrier bag is to limit dust exposure.

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_{ST}	-20	80	° C	1
Humidity	RH	5	90	%	2

Notes:

1. Storage toward the maximum temperature will accelerate color filter degradation.
2. T=25°C. Excessive humidity will degrade MTTF.

LONG TERM STORAGE

Assembled devices stored for longer than 1 year are considered to be in long-term storage. When long-term storage is anticipated, the devices in carriers should be placed into moisture proof, vacuum-sealed, anti-static bags or a similar moisture proof enclosure to prevent the deterioration of the lead pins. The moisture proof package should be stored indoors, in a dust free, enclosed environment with the following conditions:

Description	Condition
Time Limit	1 to 5 years
Temperature	20°C to 40°C
Relative Humidity	< 60%

Caution:

Long-term storage, if done improperly, may cause the lead pins to oxidize or corrode which may affect the pin solderability, or the electrical characteristics may deteriorate. When devices are stored for time periods in excess of 1 year, the pin solderability should be confirmed prior to use. Additionally, the electrical characteristics should be confirmed, as necessary, prior to use.

Note:

For devices from Long-Term Storage Image Sensor Solutions can offer a retest service for a reasonable fee.

ESD

1. This device contains limited protection against Electrostatic Discharge (ESD). Devices should be handled in accordance with strict ESD procedures for Class 2 JESD22 Human Body Model (<= 2000V) and Class B Machine Model (<=200V). Refer to Application Note MTD/PS-0224, Electrostatic Discharge Control, for proper handling and grounding procedures. This application note also contains recommendations for workplace modifications for the minimization of electrostatic discharge.
2. Devices are shipped in static-safe containers and should only be handled at static-safe workstations. See ISS Application Note MTD/PS-0224, Electrostatic Discharge Control, for handling recommendations.

SOLDERING RECOMMENDATIONS

Soldering procedure is defined as a partial heating method as follows:

a. Using a 80 Watt ESD-safe soldering iron

b. 350 °C soldering iron tip temperature for less than 3 seconds per pin

c. Allow the part to cool to room temperature

d. 350 °C soldering iron tip temperature for less than 3 seconds per pin

For circuit board repair, or de-soldering an image sensor, do not use solder suction equipment. In any instance, care should be given to minimize and eliminate electrostatic discharge.

COVER GLASS CARE AND CLEANLINESS

Devices are shipped with the cover glass region covered with a protective tape, for high volume packing. The tape should be removed upon usage.

Devices are shipped free of mobile contamination inside the package cavity. Immovable particles and scratches that are within the imager pixel area and the corresponding cover glass region directly above the pixel sites are also not allowed. The cover glass is highly susceptible to particles and other contamination.

Touching the cover glass must be avoided. See ISS Application Note MTD/PS-0237, Cover Glass Cleaning for Image Sensors, for further information.

ENVIRONMENTAL EXPOSURE

1. Do not expose to strong sun light for long periods of time. The color filters may become discolored. Long time exposures to a static high contrast scene should be avoided. The image sensor may become discolored and localized changes in response may occur from color filter aging.
2. Exposure to temperatures exceeding the absolute maximum levels should be avoided for storage and operation. Color filter performance may be degraded. Failure to do so may alter device performance and reliability.
3. Avoid sudden temperature changes.
4. Exposure to excessive humidity will affect device characteristics and should be avoided. Failure to do so may alter device performance and reliability.
5. Avoid storage of the product in the presence of dust or corrosive agents or gases.
6. Long-term storage should be avoided. Deterioration of lead solderability may occur. It is advised that the solderability of the device leads be re-inspected after an extended period of storage, over one year.

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MECHANICAL INFORMATION

VISUAL MECHANICAL SPECIFICATIONS

Laser Mark

Item	Description
Device Name	KAF-8300CE, KAF-8300XE, or KAF-8300-AXC. (Multiple versions available) See ORDERING INFORMATION section of this document
Lot Number, (If applicable)	annn – one alpha character and a 3 numeric field to designate production lot description that is used to track material through the production facility. The "nnn" field is a sequential number that can range from "000" through "999". The "a" field is also a sequential field and increments to the next alphabet character when the "nnn" field is incremented past the "999" value. NOT AVAILABLE FOR ALL VERSIONS OF THIS DEVICE. See ORDERING INFORMATION section of this document
Serial Number	nnn –a numeric field containing a maximum of three characters denoting a unique unit identifier for a device from the before mentioned production lot. The start of the sequence starts with "1". "001" is not a valid marking.

All markings shall be readable, consistent in size with no unusual debris left on the package.

Assembly/Package Integrity

Criteria	Description
Cracks	None allowed
Corner and edge chip-outs	None – exceeding 0.020" (0.50mm)
Chip-outs exposing buried metal traces	None allowed
Chip-outs, other	None allowed deeper than 50% of the ceramic layer thickness in which it resides
Scratches	None – that exceed 0.20" (0.50mm) in the major dimension and are deeper than 50% of the ceramic layer thickness in which it resides.
Lead conditions	No bent, missing, damaged, or short leads. No lead cut-off burrs exceeding 0.005" (0.13mm) in the dimension away from the lead.
Internal Appearance AndDie Condition	Local Non-UniformityLocal Non-Uniformity region (LNU) is allowed whose size is not greater than 200 um2 within the effective image area. Inspection equipment for these steps are performed using a microscope 7-50X and direct lighting (ring-light). LNU is described as a spot or streak that tends to change from light to dark in appearance as the operator rotates the part under angled lighting conditions. These non-uniformities are not visible or very hard to see under direct lighting. They tend to disappear or become much less visible under higher magnification. Conditions Other than LNU:No scratches, digs, contamination, marks, or blemishes that is attached to the die that touches 9 or more pixels in the effective image area. No loose contamination allowed when viewed at 7X and 50X magnification. No scratches, digs, contamination, marks, or blemishes greater than 10um are allowed on the bottom side of the cover glass region that is contained in or extends into the effective image area. Tools used to verify are 7X and 50X magnification.

Glass

Criteria	Description
Tilt	The reject condition is when the glass is incorrectly seated on the package or is not parallel to glass seal area. ("parallel" is defined as 0.25mm maximum end to end).
Seal	Glass seal must be greater than 50% of the width of the epoxy bond line and must not extend over the ceramic package.
Alignment	There are 4 "+" fiducials on the corners the die that must not be covered by the epoxy light shield. The 4 "+" marks must be in total view when the lid is placed looking directly down on the device with a microscope. All 4 "+" alignment marks are required to be visible in their entirety with a zero clearance tolerance.
Chips	None allowed.
Appearance	No fogged cover allowed.
Contamination	No immobile scratches, digs, contamination, marks, or blemishes are allowed on the cover glass region that is contained in or extends into the effective image area. Within the effective image area, the limit for such conditions is 10um or less. This criterion pertains to either the top or the bottom glass surface. Tools used to verify are 7X and 50X magnification.

Glass Cover Tape, for high volume packing

Criteria	Description
Placement	Per the following drawing. Shall not extend beyond the edge of the glass lid (tab excluded).
Tab Location	Located toward the pin 1/pin 40 end of the package.
Damage	Wrinkles and tears are not allowed
Bubbles	No bubbles allowed under the tape in the effective image area of the cover glass that are larger than 5mm.
Cover glass tape edge	Edges must be sealed completely
Between Cover Glass and Tape	No trapped contamination between the tape and the top of the cover glass that is within the effective image area when viewed at 7X and 50X magnification.
Contamination	After removal of the cover glass tape, no mark, blemish, or remnants of glue shall be visible on in the effective image area of the cover glass after proper removal of the cover glass tape.
Scratches	The applicating equipment will make slight scratches on the lid tapes. This is allowed

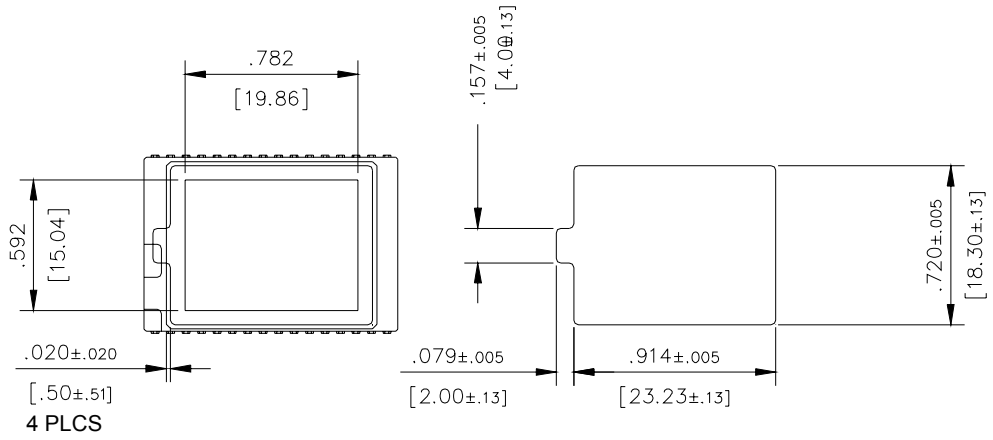
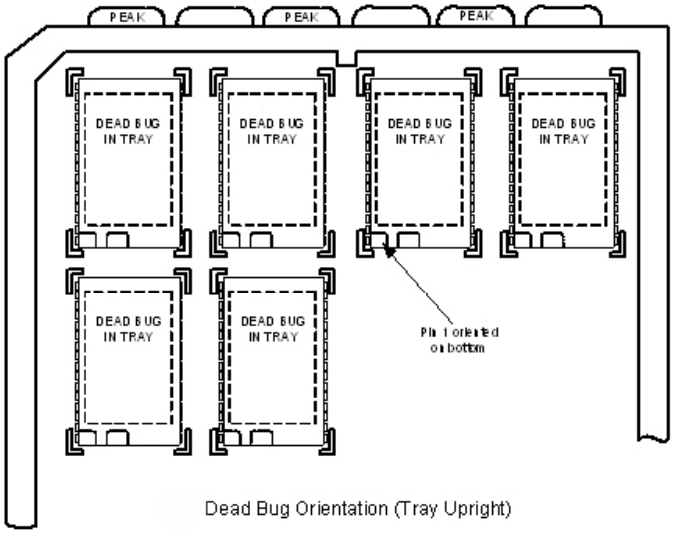


Figure 18: Cover glass protection tape, for high volume packing

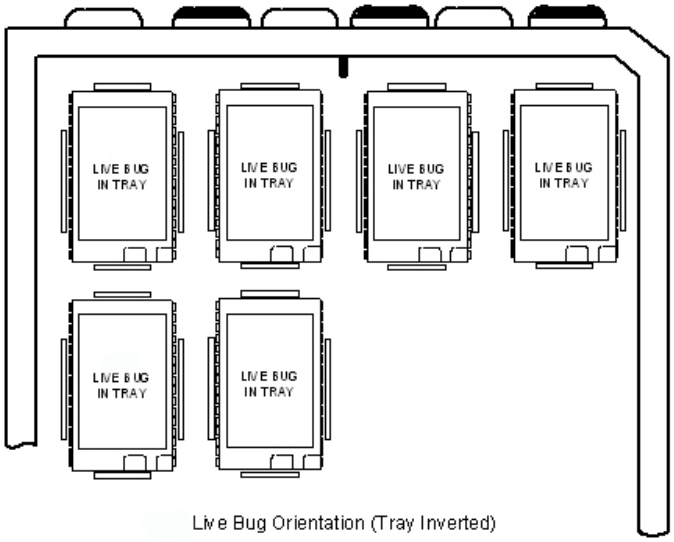
Placement in Tray, for high volume packing

Criteria	Description
Position	"Dead Bug" with leads up for an upright tray.
Pin 1 location	Faces away from the corner notch in the tray.
Number of devices per tray	32 maximum
Number of trays per shipping bundle	6 maximum
Dimension of tray, outside	135.9 mm x 315.0 mm +/- 0.25 mm

The use of high volume packing is at the discretion of the Eastman Kodak Company.



Dead Bug Orientation (Tray Upright)



Live Bug Orientation (Tray Inverted)

(Cover glass tape not shown in this drawing)

Figure 19: Package/Tray Orientation

MECHANICAL DRAWINGS

COMPLETED ASSEMBLY

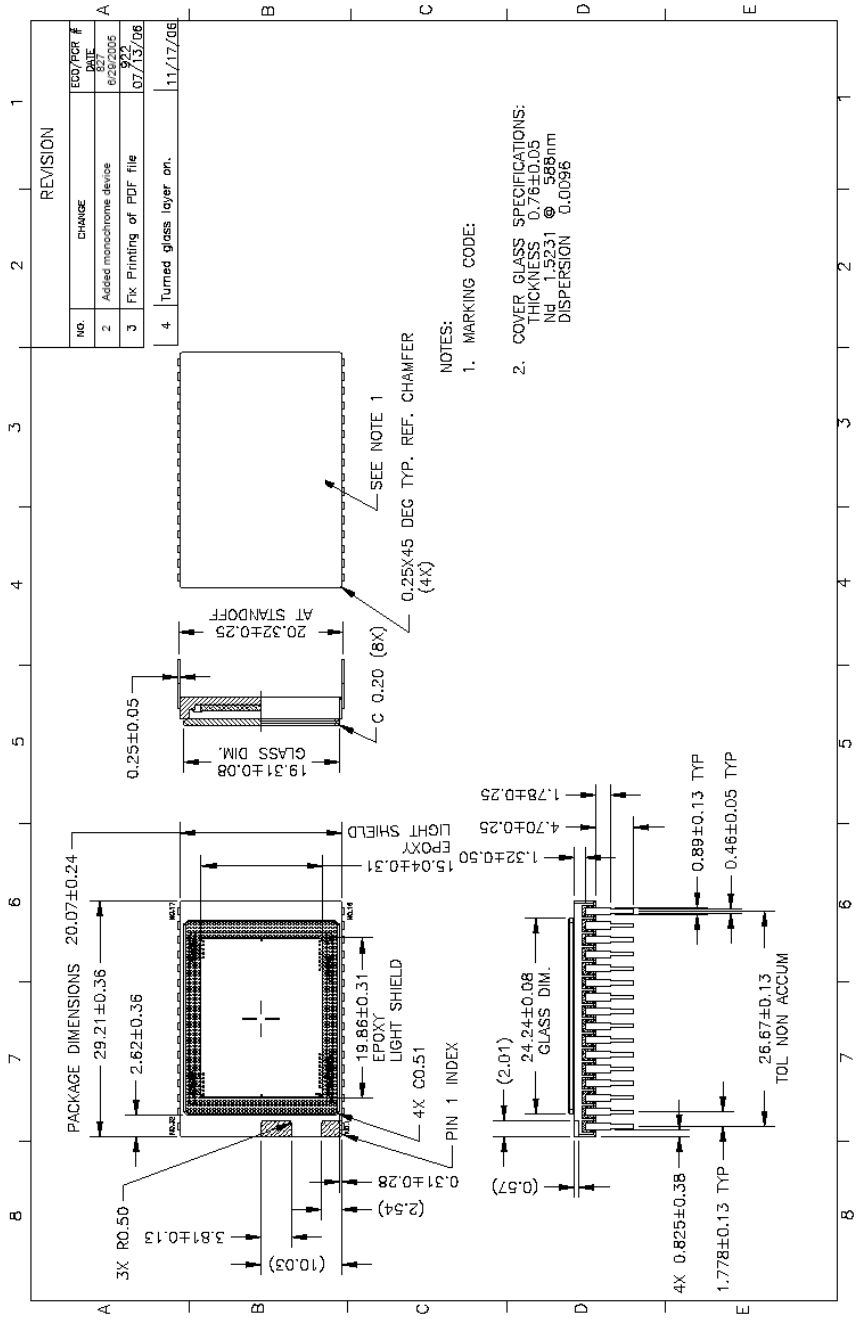


Figure 20: Completed Assembly (1 of 2)

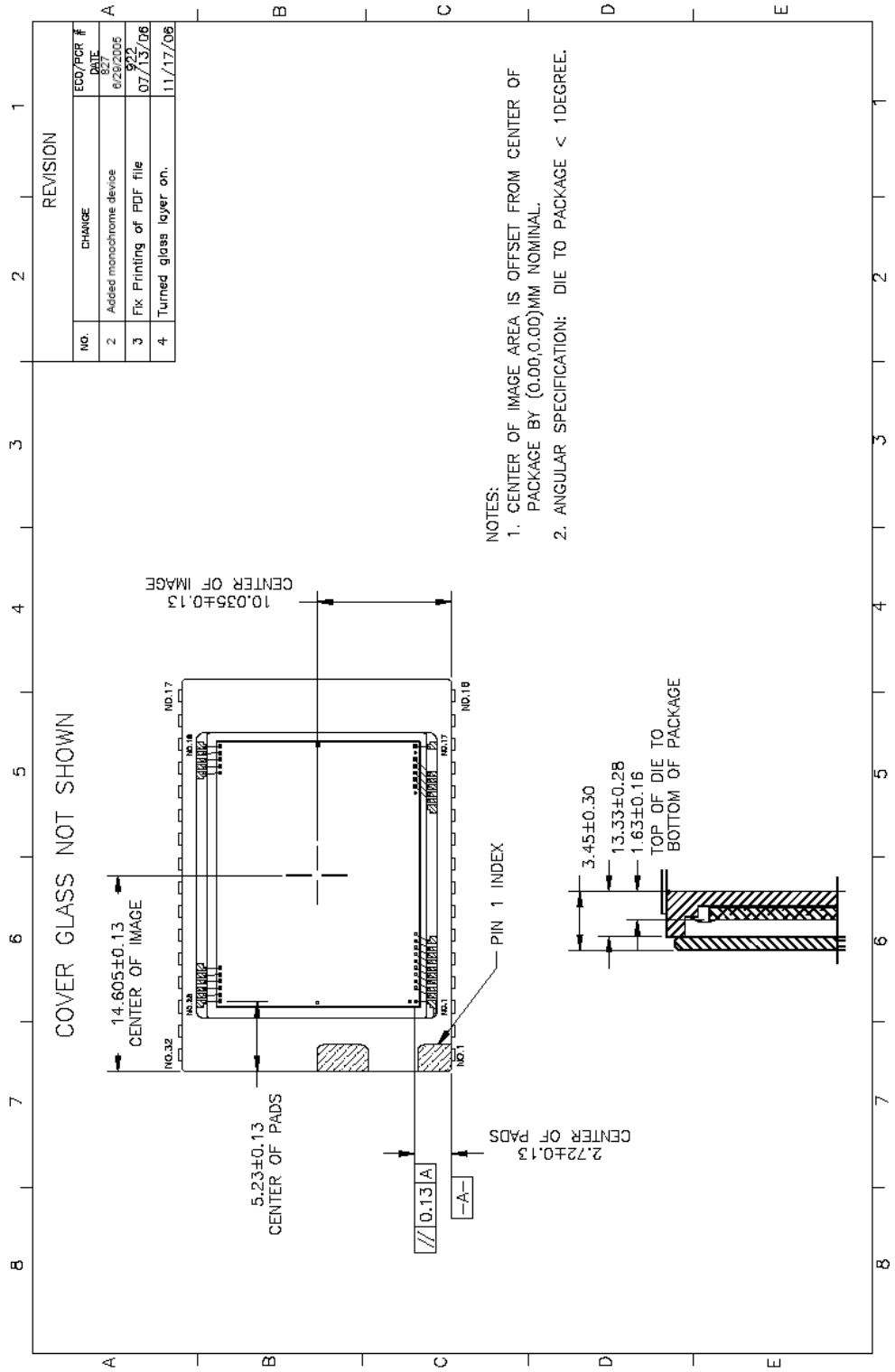


Figure 21: Completed Assembly (2 of 2)

COVER GLASS

Clear Cover Glass, AR Coated (both sides) - Specification

1. Scratch and dig: 10 micron max
2. Substrate material Schott D-263, or equivalent
3. Multilayer anti-reflective coating

Wavelength	Total Reflectance
420-450	≤ 2%
450-630	≤ 1%
630-680	≤ 2%

Clear Cover Glass – Specification

1. Scratch and dig: 10 micron max
2. Substrate material Schott D-263, or equivalent

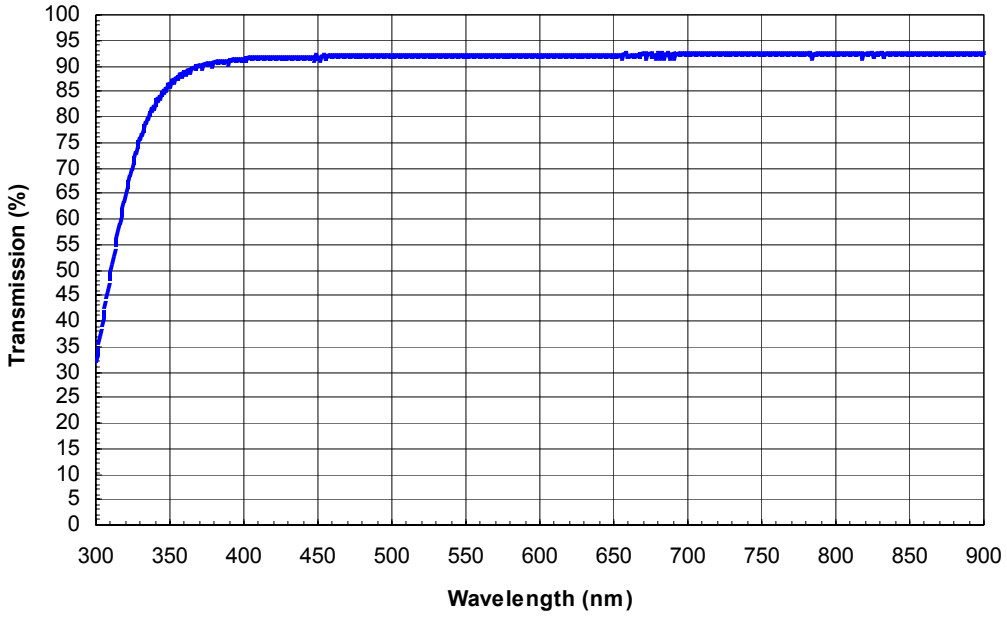


Figure 22: Clear Cover Glass Transmission, typcial

SHIPPING CONFIGURATION, HIGH VOLUME

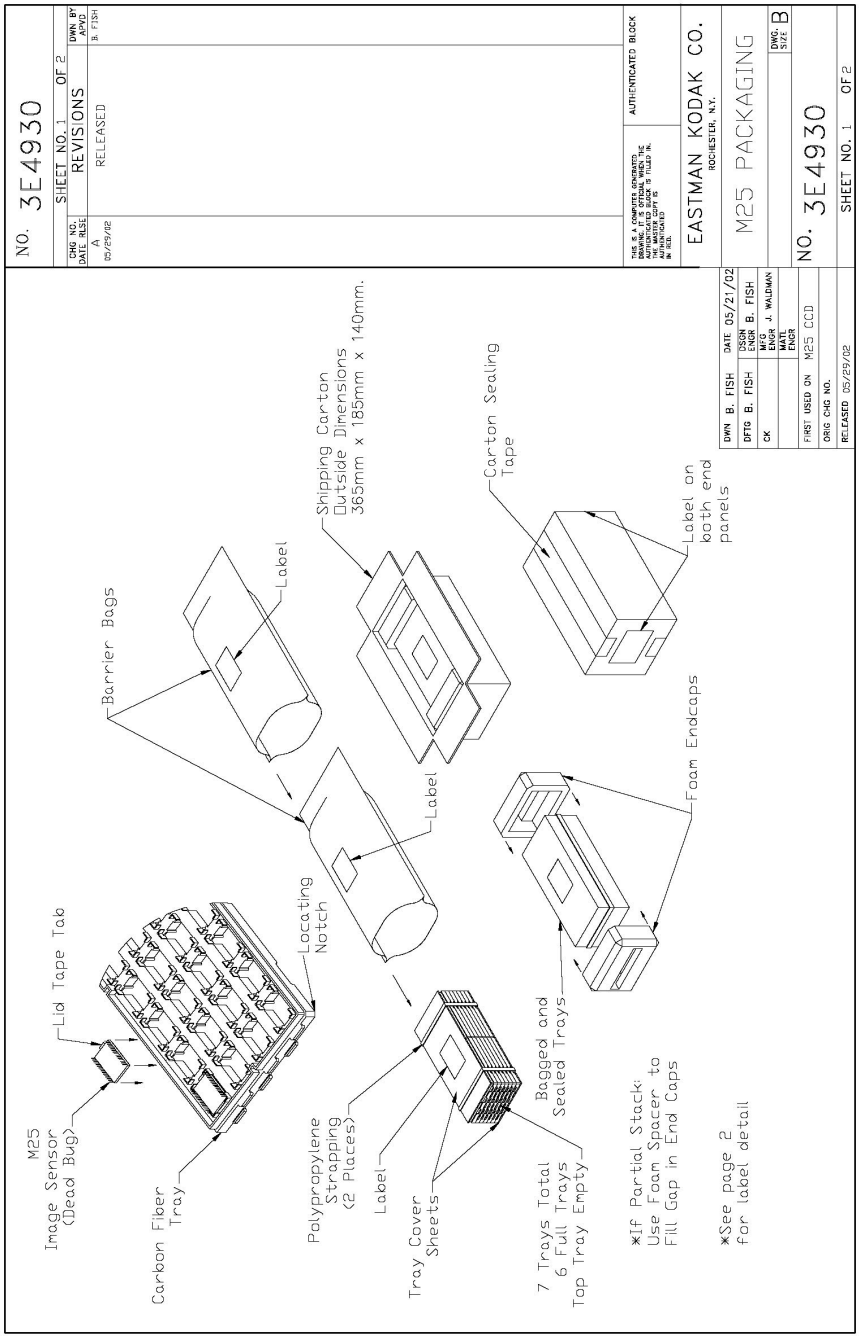


Figure 23: Packing materials configuration for high volume packing

The use of high volume packing is at the discretion of the Eastman Kodak Company.

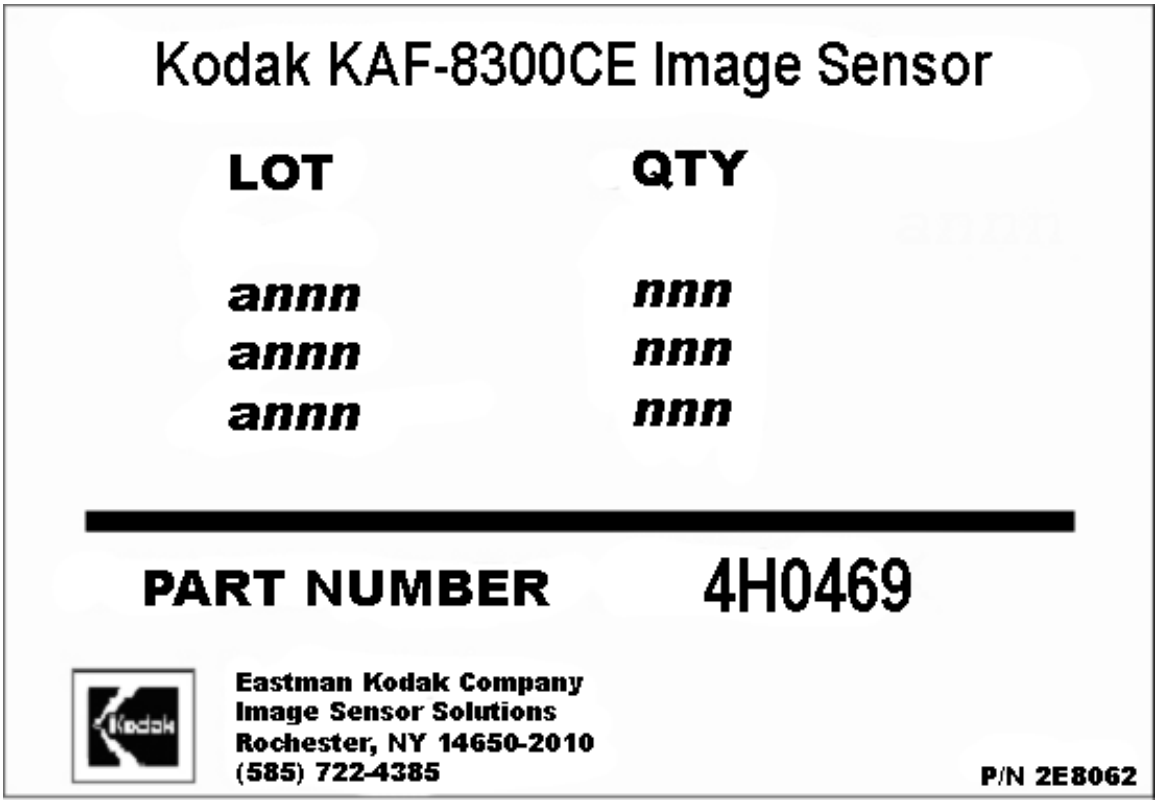


Figure 24: Packing materials, label description for high volume packing

The use of high volume packing is at the discretion of the Eastman Kodak Company.

For high volume packing, the contents of the shipping container are described on the shipping label shown above. In the "*LOT*" column, "*annn*" represents an alpha character followed by a three character numeric field that denotes the production run number contained in the shipping container. In the "*QTY*" column, the "*nnn*" represents a numeric field that represents the quantity of devices from that lot in the shipping container.

QUALITY ASSURANCE AND RELIABILITY

QUALITY STRATEGY

All image sensors will conform to the specifications stated in this document. This will be accomplished through a combination of statistical process control and inspection at key points of the production process. Typical specification limits are not guaranteed but provided as a design target. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

REPLACEMENT

All devices are warranted against failure in accordance with the terms of Terms of Sale. This does not include failure due to mechanical and electrical causes defined as the liability of the customer below.

LIABILITY OF THE SUPPLIER

A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer.

LIABILITY OF THE CUSTOMER

Damage from mechanical (scratches or breakage), or other electrical misuse of the device beyond the stated absolute maximum ratings, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

RELIABILITY

Information concerning the quality assurance and reliability testing procedures and results are available from the Image Sensor Solutions and can be supplied upon request.

TEST DATA RETENTION

Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

MECHANICAL

The device assembly drawing is provided as a reference. The device will conform to the published package tolerances.

Kodak reserves the right to change any information contained herein without notice. All information furnished by Kodak is believed to be accurate.

WARNING: LIFE SUPPORT APPLICATIONS POLICY

Kodak image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company. Product warranty is limited to replacement of defective components and does not cover injury or property or other consequential damages.

REVISION CHANGES

Revision Number	Description of Changes
1.0	Initial Release.
2.0	Add monochrome versions and the allowance of differentiating high volume packing.

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